Image Processing Apparatus and Image Processing Method Employing the Same

Cross References to Related Application

[0001] This application claims priority under 35 USC 119 of Japanese Patent Application No. 2000-99975 filed on March 31, 2000, the entire disclosure of which is incorporated herein by reference.

Background of the Invention

Field of the Invention

[0002] The present invention relates to an image processing apparatus and an image processing method employing the same which provide interpolation processing or thin-out processing for the inputted pixel data of prescribed number, i.e., for one scanning line.

Description of the Related Art

[0003] In order to enlarge or reduce an inputted image, a counter is installed to count a reference clock which controls input-output of pixel data of the image. In accordance with an enumerated value by the counter, interpolation or thin-out processing for the pixel data is performed at every pixel data of prescribed number according to a specified magnification. Such interpolation or thin-out processing conventionally handles the pixel data of one scanning line as one unit and the enumerated value by the counter is re-set at every line.

[0004] In Figures 8A and 8B of the accompanying drawings, there are shown the pixel data given the image enlargement processing (the

interpolation processing of pixel data) in conventional way as described in the above. For each prescribed number of pixels, the output time duration of one pixel datum is prolonged twice as long enough to read out the same pixel datum twice from a memory (not shown). Since an enumerated value in a counter is reset at every line in conventional way, the pixel data that require the interpolation have the same bit number in all lines as shown in Figure 8A. (In this example, the data are in 3rd bit, 7th bit, 10th bit, 15th bit,·····.) In Figure 8A, the interpolated pixels have hatching. Therefore, the pixel data after finishing the enlargement processing become like the ones shown in Figure 8B and the interpolated pixels are located exactly in the same position in whichever lines they are.

[0005] Accordingly, when the pixel data having been treated with interpolation or thin-out processing are printed on paper, there appear vertical streaks called moire in the sub-scanning direction, which causes the image degradation. Such vertical streaks are particularly noticeable in the case of pseudo gray-scale image.

[0006] Therefore, it is proposed that random numbers from a random number generator circuit are set at the counter in the beginning of each line and the position of pixels requiring interpolation or thin-out processing at each line are made to differ from each other (Japanese Patent Application, Laid Open Publication No. 4-335769). However, a random number generator circuit is prerequisite for this method, which inevitably makes the whole apparatus complex and large-scale.

Summary of the Invention

[0007] It is an object of the present invention to provide an image processing apparatus and an image processing method employing the same which suppress the emergence of vertical streaks with a simple system which does not reset an enumerated value of the counter at the

beginning of every line.

[0008] In accordance with a first aspect of the present invention, there is provided an image processing method for performing interpolation or thin-out processing to pixel data in accordance with an enumerated value in a counter counting a reference clock at every one unit which is composed of prescribed number of pixel data, characterized in that a final enumerated value in said counter for one unit is not reset but kept in the counter and a counting processing starts again at the beginning of the next unit with a consecutive enumerated value from the kept final enumerated value.

[0009] The counter keeps the final enumerated value, that is from the former unit (the former line) having the prescribed number of pixel data, instead of resetting it at the beginning of the current unit (the current line) and uses a consecutive enumerated value from said final enumerated value. Consequently, each unit (each line) has each different position of the pixel data that require the interpolation or thin-out processing, which suppresses the emergence of vertical streaks in a resulting image.

[0010] In accordance with the second aspect of the present invention, there is provided an image processing method for performing interpolation or thin-out processing to pixel data in accordance with an enumerated value of a counter counting a reference clock in a unit which is composed of a prescribed number of pixel data, characterized in that the final enumerated value of the said counter for the former unit is not reset at the beginning of the current unit if said pixel data are pseudo gray-scale but is reset if they are bi-level.

[0011] The image processing method does not reset the enumerated value of the counter at the beginning of each unit (each line) in a halftone image that likely produces vertical streaks, but resets the enumerated value of the counter at the beginning of each unit in a bi-level image that hardly produces vertical streaks. Therefore, this method allows effective processes according to the types of image.

[0012] In accordance with the third aspect of the present invention, there is provided an image processing apparatus for performing interpolation or thin-out processing to pixel image for each unit composed of the inputted prescribed number of pixel data, that includes a memory to store said inputted pixel data, a counter to count a reference clock, and a control unit to control the read of pixel data from said memory in accordance with an enumerated value of said counter and to control resetting or non-resetting of said counter at the beginning of each unit.

[0013] This image processing apparatus operates on the interpolation or thin-out processing of pixel data by controlling the read of pixel data from the memory according to the enumerated value of the counter that counts the reference clock. The control unit determines resetting or non-resetting of the enumerated value of the counter at the beginning of each unit. The control unit does not reset the enumerated value of the counter at the beginning of the unit in order to put the pixels that need the interpolation or thin-out processing in different positions, so that the emergence of vertical streaks may be suppressed in a resulting image.

Brief Description of the Several Views of the Drawings

[0014] Figure 1 is a schematic diagram showing the flow of pixel data and clock signals in an enlargement processing in accordance with the present invention.

[0015] Figure 2 illustrates a timing chart of the enlargement processing shown in Figure 1.

[0016] Figure 3A illustrates initial parts of pixel data in three scanning lines when the enlargement processing (the interpolation processing of pixel data) is carried out in accordance with the present invention.

[0017] Figure 3B illustrates a diagram of the three lines after the

enlargement processing.

[0018] Figure 4 is a schematic diagram showing the flow of pixel data and clock signals in a reduction processing in accordance with the present invention.

[0019] Figure 5 is a timing chart of the reduction processing shown in Figure 4.

[0020] Figure 6 is similar to Figure 1 and illustrates the flow of pixel data and clock signals in the enlargement processing together with a reset signal.

[0021] Figure 7 is a flowchart showing the processing of a reset control device used in Figure 6.

[0022] Figure 8A shows the initial part of pixel data in three lines when the enlargement processing (the interpolation processing of pixel data) is carried out in accordance with the conventional way.

[0023] Figure 8B shows the three lines after the conventional enlargement processing.

Detailed Description of the Invention

[0024] Embodiments of the present invention will now be described with reference to the accompanying drawings.

[0025] The first embodiment: Enlargement processing

[0026] Referring to Figures 1 and 2, a line FIFO (First-Input First-Output) buffer 1 inputs pixel data Di one by one in synchronization with the input clock signals CLKi and outputs pixel data Do one by one in synchronization with the output clock signals CLKo. A counter 2 counts

the pulses of the input clock signal CLKi, that is to be the reference clock, and outputs the enumerated value to a clock thin-out circuit 3. A register 4, which keeps the timing data showing which pixel data should be interpolated in accordance with the set scaling, outputs the timing data to the clock thin-out circuit 3. The clock thin-out circuit 3 generates the output clock signal CLKo by thinning out the input clock signal CLKi in accordance with the timing data and outputs it to the line FIFO buffer 1.

[0027] The pixel data Di are inputted to the line FIFO buffer 1 successively in synchronization with the input clock signal CLKi. The clock thin-out circuit 3 generates the output clock signal CLKo from the input clock signal CLKi by thinning out 3rd clock, 5th clock, 8th clock and other number of clocks in the input clock signal, and outputs it to the line FIFO buffer 1. The timing data that is the base of the thin-out pattern is inputted from the register 4 and the enumerated value of the input clock signal CLKi is inputted from the counter 2. The pixel data Do is output from the line FIFO buffer 1 successively in synchronization with the output clock signal CLKo. Those pixel data Do that should be interpolated are prolonged twice in the time so that said pixel data can be read out again. It allows the enlargement processing with the scaling factor 8/5=160%.

[0028] The enumerated value is reset by inputting the reset signal into the counter 2 every time the measurement of one line is over in conventional enlargement processing. Every line has, therefore, all the same interpolation patterns as described before (see Figures 8A and 8B), which generates the vertical streaks that are the cause the image degradation.

[0029] In the present invention, the reset signal like the above is not inputted into the counter 2 but a consecutive enumerated value from the stored final enumerated value of the prior line is output to the clock thin-out circuit 3.

[0030] Figures 3A and 3B are diagrams showing the initial part of a pixel data line when the enlargement processing (the interpolation processing of pixel data) is carried out in accordance with the present invention. As shown in Figure 3A, since an enumerated value in the counter is not reset at every line in the present invention, every line has its own bit numeral numbers different from other lines for the pixels (with hatching) requiring the interpolation. Consequently, the pixel data after finishing the enlargement processing become ones like shown in Figure 3B and the resulting pixels are positioned randomly, which suppresses the emergence of vertical streaks.

[0031] In the above example, the maximum value M in the counter 2 is set smaller than N, the number of the pixel data in a line (M<N). When amounting to the value M, the enumerated value of the counter 2 is set back to one by the next input clock signal CLKi. In other words, the counter 2 counts values cyclically in one scanning line. The scaling factor should be programmed so as to satisfy the condition that N is not dividable by M. In the example shown in Figure 3A, N and M are determined such that N is divided by M with the remainder, two.

[0032] The second embodiment: Reduction processing

[0033] Figure 4 is a diagram showing the flow of pixel data and clock signals in the case that the present invention is applied to reduction processing and Figure 5 is a timing chart. Similar reference numerals are used in Figures 1 through 5 to designate similar elements. The line FIFO buffer 1 inputs the pixel data Di one by one in synchronization with the input clock signal CLKi, and outputs the pixel data Do one by one in synchronization with the output clock signal CLKo. The counter 2 counts the pulses of the output clock signal CLKo, that is to be the reference clock, and outputs the enumerated value to the clock thin-out circuit 3. The register 4, which stores the timing data revealing which pixel data should be thinned out in accordance with the given scaling, outputs the timing data to the clock thin-out circuit 3. The clock thin-out circuit 3 generates the input clock signal CLKi by thinning out the output

clock signal CLKo in accordance with the timing data and outputs it to the line FIFO buffer 1.

[0034] The pixel data Di are inputted to the line FIFO buffer 1 successively in synchronization with the input clock signal CLKi. Since the input clock signal CLKi is generated in the clock thin-out circuit 3 by thinning out 3rd clock, 5th clock, 8th clock…… of the output clock signals CLKo, the 3rd, 5th, 8th …… pixel data Di are not inputted into the line FIFO buffer 1. The pixel data without the above thinned out pixel data are output as the pixel data Do. The timing data that is the base of the thin-out pattern is inputted from the register 4, and the enumerated value of the output clock signal CLKo are inputted from the counter 2. The pixel data which need thinning out are not read out by thinning out the input clock signal CLKi. It allows the reduction processing with the scaling factor 5/8=62.5%.

[0035] The conventional way inputs the reset signal into the counter 2 at every line and resets the enumerated value even in the reduction processing like the above. As a result, the vertical streaks that are the cause of picture degradation are generated. In the present prevention, since the enumerated value in the counter 2 is not reset at every line like the case in the enlargement processing, every line has its own bit numeral numbers different from other lines for the pixels requiring the thinning-out, that is, the thinned out pixels are positioned in random, which suppresses the emergence of vertical streaks.

[0036] Incidentally, if a value N designates the number of pixels in one line, a value M designates the maximum value counted by the counter 2 and N (mod M)$\equiv$0 is proved, the enumerated value in the counter 2 is reset every time at the beginning of a line even without the input of reset signal. The scaling is set in order not to provide such condition.

[0037] The above-mentioned vertical streaks are seen conspicuously in the pseudo gray-scale image but not in the bi-level image. Consequently, it is efficient that the enumerated value in the counter 2 is not reset every

time at the beginning of a line in the pseudo gray-scale image but reset in the bi-level image like the conventional way. Examples of such conditions are described as a third embodiment.

[0038] The third embodiment: Reset control and non-reset control

[0039] Figure 6 is a schematic diagram showing the flow of pixel data, clock signals, and reset signals on condition that the first embodiment (enlargement processing) has an additional control function of resetting. Elements and parts in Figure 6 common to the ones in Figure 1 are given the same numbers or marks as in Figure 1 and the explanation of them are abbreviated.

[0040] A reset control unit 5 outputs a reset signal to the counter 2 at the end of every line if the image is not a pseudo gray-scale image. Receiving said reset signal, the counter 2 resets its own enumerated value at the beginning of a line.

[0041] Figure 7 illustrates a flowchart showing the operations of the reset control unit 5. The reset control unit 5 receives an image distinction signal (step S1) and judges whether the present image is a pseudo gray-scale image or not in accordance with said signal (step S2). Unless the image is a pseudo gray image that likely produces vertical streaks (step S2: No), the reset control unit 5 outputs a reset signal to the counter 2 (step S4) every time it detects the end of a line (step S3: YES). Outputting of the reset signal continues until all lines are processed (step S5: YES). If the image is ,on the other hand, a pseudo gray-scale image (S2: YES), the reset control unit 5 does not output a reset signal.

[0042] The above is the case where the reset control unit is added to the first embodiment. It is needless to say that the same control unit can be applied to the second embodiment (the reduction processing).